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EXAMINER	
MILLS, DONALD L	
ART UNIT	PAPER NUMBER
2662	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/585,744	MIAO, KAI	
	Examiner	Art Unit	
	Donald L Mills	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

The specification lacks a Brief Summary of the Invention section, which is separate and distinct from the abstract and directed toward the invention rather than the disclosure as a whole.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 11-13, 15, 22, 23, 25, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by De Prycker (US 4,817,085).

Regarding claim 11, De Prycker discloses a system, which comprises:

Receiving a packet (Referring to Figure 1, a packet is received by the destination interface circuit **NAI**. See column 3, lines 51-52.)

Reading information in the packet and ascertaining therefrom a delay incurred by the packet in traversing the network (Referring to Figure 1, the packets are read by **EM2.** Where the

packets have a random delay, **t0**, **t1**, **tk**, ... based upon their path through the **PSN**. See column 3, lines 54-57.)

Comparing the delay ascertained to a dynamically adapted optimal delay (Referring to Figure 1, **to + Tm = T2**, inherently dynamically adapted by **Tm** in order to smooth the influence of random network delay. See column 4, lines 12-13.)

Delaying use of the packet to reconstruct a signal by a calculated amount of time sufficient to make the calculated amount of time plus the ascertained delay substantially equal to the optimal delay (Referring to Figures 1 and 2, the packet is delayed for reconstruction by a calculated delay **Tm** and random delay **to** equal to the delay time **T2**. See column 4, lines 11-12 and column 6, lines 8-11.)

Regarding claim 12, De Prycker discloses *setting the optimal delay at an amount equal to a minimum delay required to cause a specified probability of packet loss* (Referring to Figures 1 and 2, **Tr** is set equal to **T2** or larger so that no packets will be lost. See column 6, lines 10-12.)

Regarding claim 13, De Prycker discloses *the required minimum delay is recalculated every Nth packet, where N is a positive integer* (Referring to Figures 1 and 2, the first packet **DP0** is submitted to a total delay **T2**. See column 4, lines 11-12.)

Regarding claim 15, De Prycker discloses a system, which comprises:

A CPU for calculating a delay to which each of a plurality of received packets should be subjected (Referring to Figure 1, the common computer **CC** controls the timing circuit **TC** for controlling the delay of the packets. See column 3, lines 9-11 and lines 64-66.)

A buffer for storing the received packets (Referring to Figure 1, buffer unit **BU** stores the received packets. See column 3, lines 60-61.)

A timer for subjecting each packet to a calculated delay (Referring to Figure 1, the timer circuit **TC** counts a time **Tm**. See column 3, lines 65-66,) *that equals a dynamically adapted optimal delay minus a network delay experienced by the packet* (Referring to Figures 1 and 2, the first packet **DP0** is submitted to a total delay **T2**, that includes a random delay **t0**. The difference between the total delay and random delay is inherent in the mathematical equation **T2**, dynamically adapted by **Tm** in order to smooth the influence of random network delay, = **to** + **Tm**. See column 3, line 56 and column 4, lines 12-13,) *unless such calculated delay exceeds a predetermined maximum, in which case the predetermined maximum is utilized as the calculated delay* (Referring to Figures 1 and 2, the buffer **BU** has been given a maximum size corresponding to a delay time **Tr** such that **Tr** remains larger than or equal to **T2**. See column 6, lines 9-11.)

Regarding claim 22, De Prycker discloses a system, which comprises:

A signal processor for calculating a delay experienced by each of a plurality of packets through a data network (Referring to Figure 1, the packets are read by **EM2.** Where the packets have a random delay, **t0**, **t1**, **tk**, ... based upon their path through the **PSN**. See column 3, lines 54-57.)

A buffer system for delaying further conveyance of each of the packets by an amount of time dependent upon (Referring to Figures 1 and 2, the buffer **BU** has been given a maximum size corresponding to a delay time **Tr**, which is equal to **T2**, so that the packets are delayed. See column 6, lines 9-11,) *(1) a probability distribution updated in response to receipt and processing of selected ones of each of the packets* (The probability density function is generated in response to the first packet **DP0**. See column 6, lines 30,) *and (2) the calculated delay*

(Referring to Figure 1, **T2=to+Tm**, where **to** is the random delay through the network. See column 5, lines 59-67.)

Regarding claim 23, De Prycker discloses *the buffer system arranged to delay further conveyance by an amount also dependant upon a prestored maximum* (Referring to Figures 1 and 2, buffer unit **BU** can store packets for a longer time equal to **Tr** as a maximum size. See column 4, lines 14-16.)

Regarding claim 25, De Prycker discloses *an interrupt generator for generating an interrupt when the amount of time for each packet expires* (Referring to Figures 1 and 2, discarding is performed when a packet **DPK** does not arrive in time. See column 4, lines 65-67.)

Regarding claim 26, De Prycker discloses *a poller for sequentially polling each of a plurality of storage locations within the buffer system to determine if a packet within the storage location is to be further conveyed* (Referring to Figures 1 and 2, a packet search circuit **PSC** searches in the buffer unit **BU** for the first packet **DP0** and transfers it to the depacketizer circuit **DPA** at the appropriate clock interval and then searches for the next packet, if the packet is not available it is discarded (See column 3, lines 66-68 and column 4, lines 1-8.)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-10 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over De Prycker (US 4,817,085).

Regarding claim 1, De Prycker discloses a system, which comprises a *storage location for storing packets received from a network* (Referring to Figure 1, buffer unit **BU**, exchange memory **EM2**, and package recognition circuit **PRC** store packets received from the PSN. See column 3, lines 7-9.) *A system for dynamically calculating a probability distribution associated with network delays for plural packets* (The system calculates the probability density function based upon the delay required for proper transmission through the network for the packets. See column 6, line30.) And, a *CPU for calculating, based upon the dynamically calculated probability distribution, a delay associated with the storage location,* (The computer **CC** controls the distribution, which inherently includes the calculation of the probability density function and the buffer delay associated with the packet. See column 3, lines 65-67 and column 4, lines 11-15,) *and for causing a packet in the storage location to be transmitted out of the storage location after an amount of time equal to the delay associated with the storage location* (The packets are transmitted from the **BU** and **PRC** according to the total delay suffered by the packet which is dependent on buffer delay. See column 3, lines 65-67 and column 4, lines 11-15.) De Prycker does not disclose *a plurality of storage locations.*

De Prycker teaches a system where the delay is calculated based upon a predetermined probability that the errors in the delayed packets, which are stored in a buffer, are always less than a predetermined value (See column 2, lines 3-6.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize multiple buffers. One of ordinary skill in the art at the time the invention

was made would have been motivated to do so in order to support multiple data inputs from different sources and increase system efficiency by eliminating inefficient large buffers. In addition, unexpected results are not produced.

Regarding claim 2, the primary reference further teaches a system wherein *the CPU calculates a difference between the optimal delay permissible to guarantee a predetermined probability of packet loss, and an actual delay experienced by the packet for which the calculation is being done* (Referring to Figures 1 and 2, the first packet **DP0** is submitted to a total delay **T2**, which guarantees a predetermined probability of loss, that includes a random delay **t0**. The difference between the total delay and random delay is inherent in the mathematical equation **T2=to+Tm**. See column 3, line 56 and column 4, lines 12-13.)

Regarding claims 3 and 4, the primary reference further teaches a *probability distribution is updated every Nth packet received, where N is a positive integer (Claim 3)/where N is 1 (Claim 4)* (Referring to Figures 1 and 2, the probability distribution calculation includes packets **DP0, DP1, DPk**. See column 4, lines 33-45.)

Regarding claim 5, De Prycker discloses: *a Central Processing Unit (CPU) for causing packets arriving from a network at the apparatus to be stored in the buffer* (Referring to Figure 1, the common computer CC controls the storage of packets in buffer unit **BU**. See column 3, lines 59-61,) *the CPU also being arranged to calculate, upon receipt of every Nth packet or data, an optimal delay beyond which a packet will be lost* (When the whole packet **DPk** does not arrive in time it is discarded. See column 4, lines 65-66.) And, *a timer for causing each packet to incur an added delay* (The timer circuit **TC** counts a time **Tm**. See column 3, lines 65-66,) *at the gateway of the difference between the calculated optimal delay and the actual delay*

experienced by each packet (Referring to Figures 1 and 2, the first packet **DP0** is submitted to a total delay **T2**, which guarantees a predetermined probability of loss, that includes a random delay **to**. The difference between the total delay and random delay is inherent in the mathematical equation **T2=to+Tm**. See column 3, line 56 and column 4, lines 12-13.) De Prycker does not disclose *plural buffers*.

De Prycker teaches a system where the delay is calculated based upon a predetermined probability that the errors in the delayed packets, which are stored in a buffer, are always less than a predetermined value (See column 2, lines 3-6.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize multiple buffers. One of ordinary skill in the art at the time the invention was made would have been motivated to do so in order to support multiple data inputs from different sources and increase system efficiency by eliminating inefficient large buffers. In addition, unexpected results are not produced.

Regarding claims 6 and 7, the primary reference further teaches *wherein N is greater than 1 (Claim 6)/wherein N is 1 (Claim 7)* (Referring to Figures 1 and 2, the probability distribution calculation includes packets **DP0, DP1, DPk**. See column 4, lines 33-45.)

Regarding claim 8, the primary reference further teaches *a network interface card for receiving signals from the data network* (Referring to Figure 1, the sender/receiver circuit **SEND/REC** is coupled to the packet switching network **PSN**. See column 2, lines 61-64.)

Regarding claim 9 as explained above in the rejection statement of claim 5, De Prycker discloses all the claim limitations of claim 5 (parent claim). De Prycker does not disclose *the CPU as a Digital Signal Processing (DSP) chip that performs DSP and control functions*.

De Prycker teaches a user circuit that generates and receives a continuous bit-stream, which may be constituted by voice, video, or other data or a mixture thereof; which, inherently includes an A/D converter in order to digitize the traffic for communication across the network (See column 3, lines 16-19.) De Prycker further teaches a common computer **CC**, which controls the system (See column 3, lines 3-6.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the functions of the user circuit and common computer into one processor. One of ordinary skill in the art at the time the invention was made would have been motivated to do so in order to increase the inefficiency in which the signals are processed. In addition, in so doing unexpected results are not produced.

Regarding claim 10 as explained above in the rejection statement of claim 5, De Prycker discloses all the claim limitations of claim 5 (parent claim). De Prycker does not disclose the *network interface card as implementing the G.723 or G.729 standard.*

De Prycker teaches a sender/receiver circuit **SEND/REC** that is coupled to the packet switching network **PSN** (See column 2, lines 61-64.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the G.723 or G.729 standard in the sender/receiver circuit. One of ordinary skill in the art at the time the invention was made would have been motivated to do so because the G.723 and G.729 standards are well known in the art.

Regarding claim 24 as explained above in the rejection statement of claim 22, De Prycker discloses all the claim limitations of claim 22 (parent claim). De Prycker does not disclose the *signal processor as programmed to use a recursive algorithm.*

De Prycker teaches a system where the delay is calculated based upon a predetermined probability that the errors in the delayed packets are always less than a predetermined value, which is based upon network delay (See column 2, lines 3-6.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the calculation of network delay in a recursive algorithm. One of ordinary skill in the art at the time the invention was made would have been motivated to do so because recursive algorithms are well known in the art.

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over De Prycker (US 4,817,085) in view of Jain (US 6,259,677 B1).

Regarding claim 14 as explained above in the rejection statement of claim 11, De Prycker discloses all of the claim limitations of claim 11. De Prycker does not disclose *comparing said required minimum delay to a predetermined value each time said required minimum delay is recalculated, and, if said recalculated required minimum delay exceeds said predetermined value, assigning said required minimum delay to be said predetermined value instead of said recalculated required minimum delay.*

Jain teaches a method of receiving and playing packetized real-time data which comprises initializing a packet transmission fixed delay and a playout delay estimate; a packet delay is calculated for each packet as it is received; and the fixed delay estimate is adjusted downwards if the fixed delay estimate is greater than the packet delay for the current packet (See column 3, lines 60-67.) Jain further teaches when packets are received very late they are marked so that they will not affect playout delay estimates (See column 6, lines 48-49.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Jain in the system of De Prycker. One of ordinary skill in the art would have been motivated to do so in order to accurately follow the jitter envelope of the variable packet delays and adjust playout time accordingly for better performance at connection startup as taught by Jain (See column 3, lines 31-35.)

7. Claims 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain (US 6,259,677 B1) in view of Lauret (US 2002/0191645A1).

Regarding claim 16, Jain discloses a dynamic jitter management system for voice over IP and Real-Time data, which comprises:

Receiving a first packet at a receiving gateway (A gateway operates as a receiver, buffering voice packets. See column 4, lines 46-47.)

Fixing any synchronization error between a transmitting gateway and the receiving gateway to a reasonable value of a delay the packet experienced in traversing a network (Referring to Figure 2, the first delay, d_f, represents the minimum travel time that a packet will incur in the network as it passes from sender to receiver, used for determining proper playout time for synchronizing real-time traffic. See column 4, lines 58-60.) Jain does not disclose *setting a clock at the receiving gateway to a value equal to a time stamp contained within the first packet plus the reasonable value.*

Lauret teaches setting the clock frequency at the ATM receiver to **SRTSreceived** and **D** (See page 3, section 54, lines 1-7.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the clock setting method of Lauret in the system of Jain. One of ordinary skill in the art would have been motivated to so in order to more accurately assess the real clock offset and increase the accuracy of the packet jitter estimation for real-time data as taught by Lauret (See paragraph 2, lines 12-14.).

Regarding claim 17, the primary reference further teaches *receiving packets in addition to said first packet, reading a time stamp from said additional packets, calculating network delay for each of said additional packets based upon said clock at said receiving gateway and said timestamp from each of said additional packets* (Referring to Figure 5, summer **40** computes a raw packet delay n_i for each packet i as the difference between the send timestamp ts_i and a receive timestamp tr_r. Receive timestamp tr_i is computed from a receive clock. See column 5, lines 48-50 and 55-56.)

Regarding claim 18, the primary reference further teaches *updating a probability distribution function indicative of network delays after receipt of every Nth packet, where N is a positive integer* (Referring to Figure 5, a packet jitter value is computed for each packet by subtracting the fixed delay from the timestamp difference for that sample. See column 6, lines 36-38.)

Regarding claim 19 as explained above in the rejection statement of claim 16, Jain and Lauret disclose all of the claim limitations of claim 16 (parent claim). Jain does not disclose *wherein said updating is done using a recursive algorithm.*

Jain teaches a dynamic jitter management system for voice over IP and Real-Time data, which comprises a variable delay estimator which calculates packet jitter value for each packet (See column 6, lines 6-7.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the calculation of packet jitter in a recursive algorithm. One of ordinary skill in the art at the time the invention was made would have been motivated to do so because recursive algorithms are well known in the art.

Regarding claim 20, the primary reference further teaches *wherein said updating further comprises recalculating a buffer latency* (Referring to Figure 5, packet jitter values are fed to adaptive playout delay estimator **46**, which in turn feeds playout delay values to playout buffer control **48**, inherently processed for each packet. See column 6, lines 11-13.)

Regarding claim 21, the primary reference further teaches *wherein said buffer latency is assigned a value different from the recalculated buffer latency if and only if said recalculated buffer latency exceeds a predetermined value* (Referring to Figure 5, when the packet arrives before the minimum arrival time predicted by the current fixed delay estimate, the fixed delay estimate is set to the timestamp difference and the packet's jitter is reset to zero, directly affecting the playout delay values for the playout buffer. See column 6, lines 39-43.)

Response to Arguments

8. Applicant's arguments filed December 29, 2003 have been fully considered but they are not persuasive.

In response to applicant's argument based on 35 USC § 102 and 103(a), regarding claims 1, 5, 11, and 15, applicant states De Prycker does not teach or disclose a *dynamically adapted optimal delay.* However, De Prycker discloses a total delay **T2**, which is equal to the random delay of arriving packets, **t0**, **t1**, etc, and smoothing delay, **Tm**. Thereby, dynamically adapting the total delay according to the random and smoothing delay. Regarding claims 22 and 24, applicant states De Prycker does not teach or disclose *updating in response to receipt and processing of selected ones of each of the packets.* However, De Prycker discloses delaying a first packet **DP0** by a total delay **T2** based upon the first packet's random delay **t0**. The value of **T2** is calculated based upon the first of several received packets random delay, this statement corresponds to updating based upon a selected packet.

Applicant's arguments with respect to claims 16-21 have been considered but are moot in view of the new grounds of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donald L Mills whose telephone number is 703-305-7869. The examiner can normally be reached on 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 703-305-4744. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donald L Mills

March 3, 2004

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